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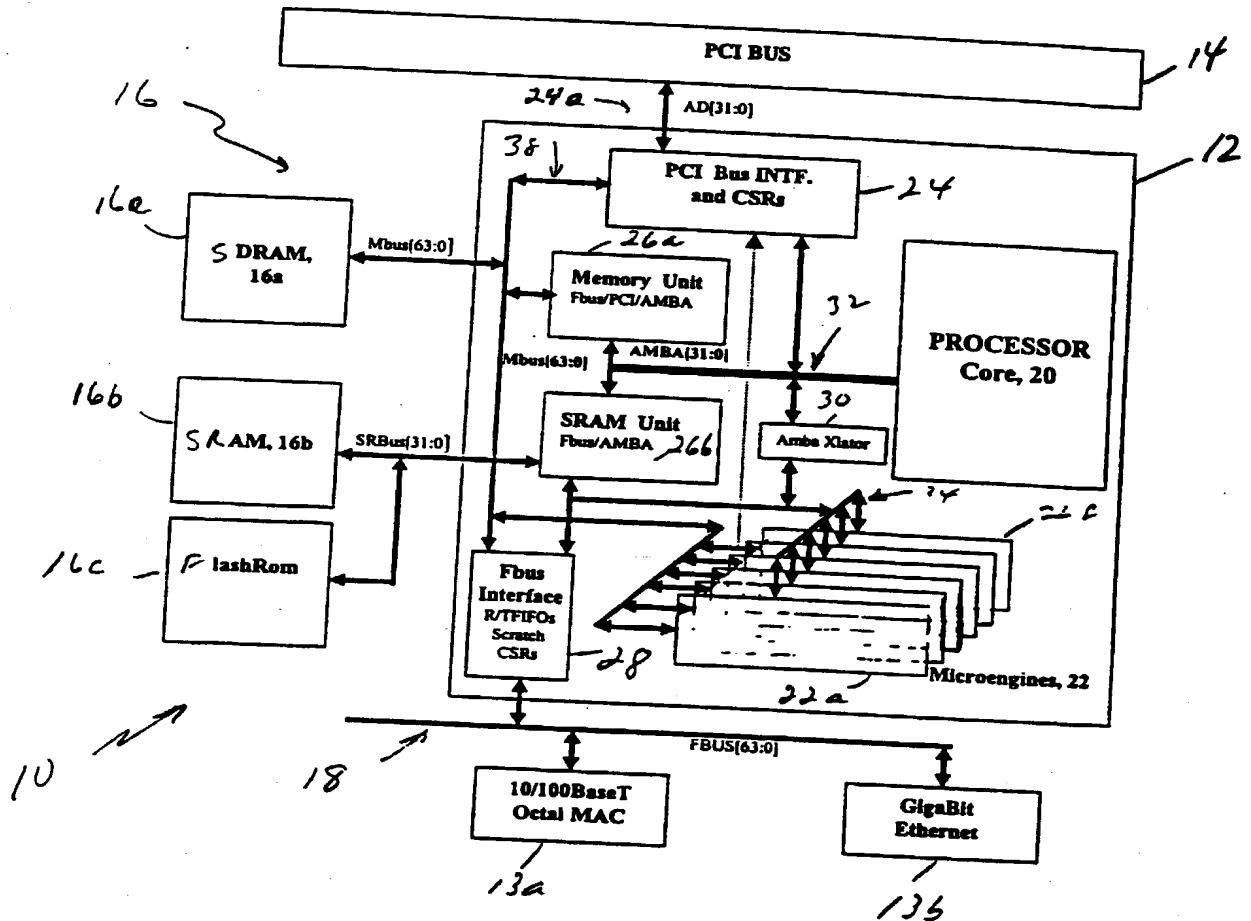


FIG. 1

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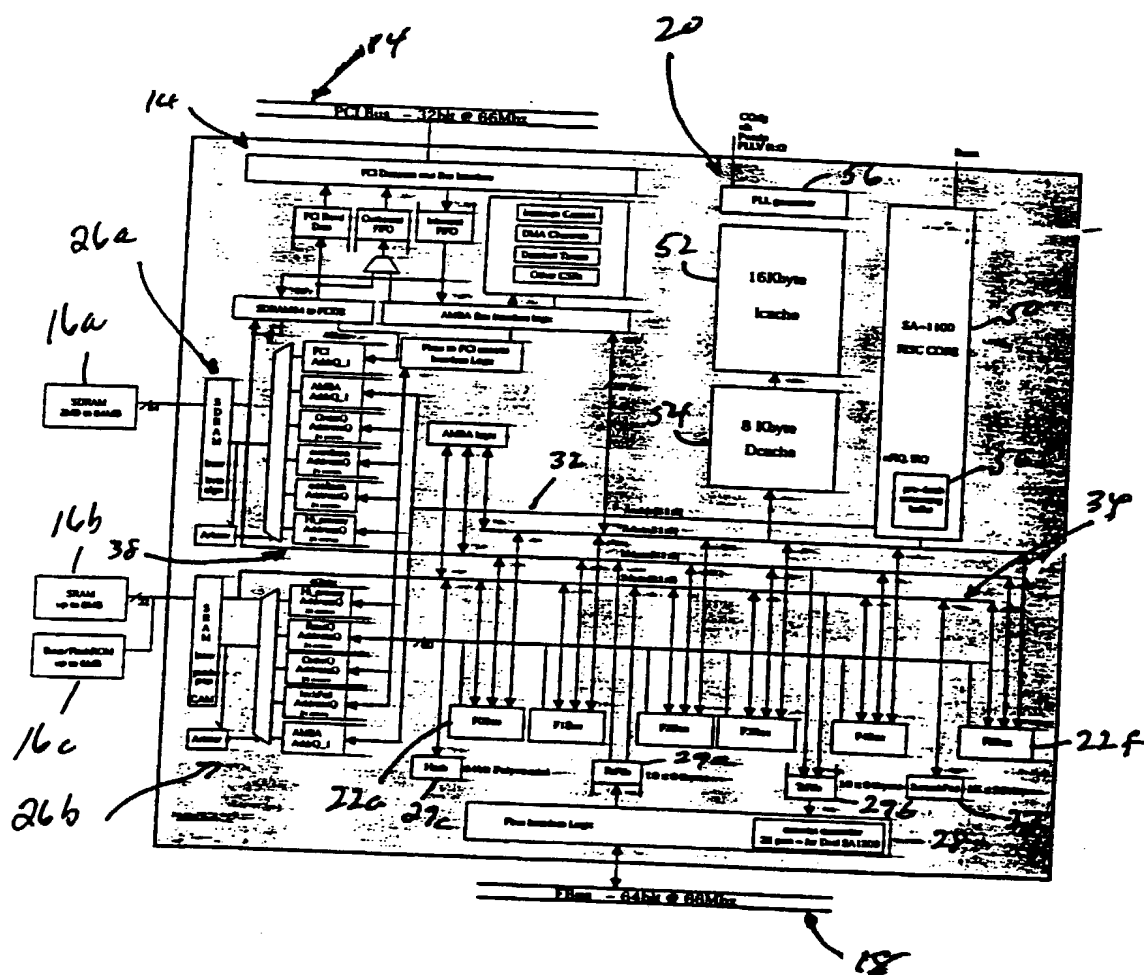


FIG. 2

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Matter No.: 10559-307US1  
Applicant(s): Gilbert Wolrich et al.  
BRANCH INSTRUCTION FOR MULTITHREADED  
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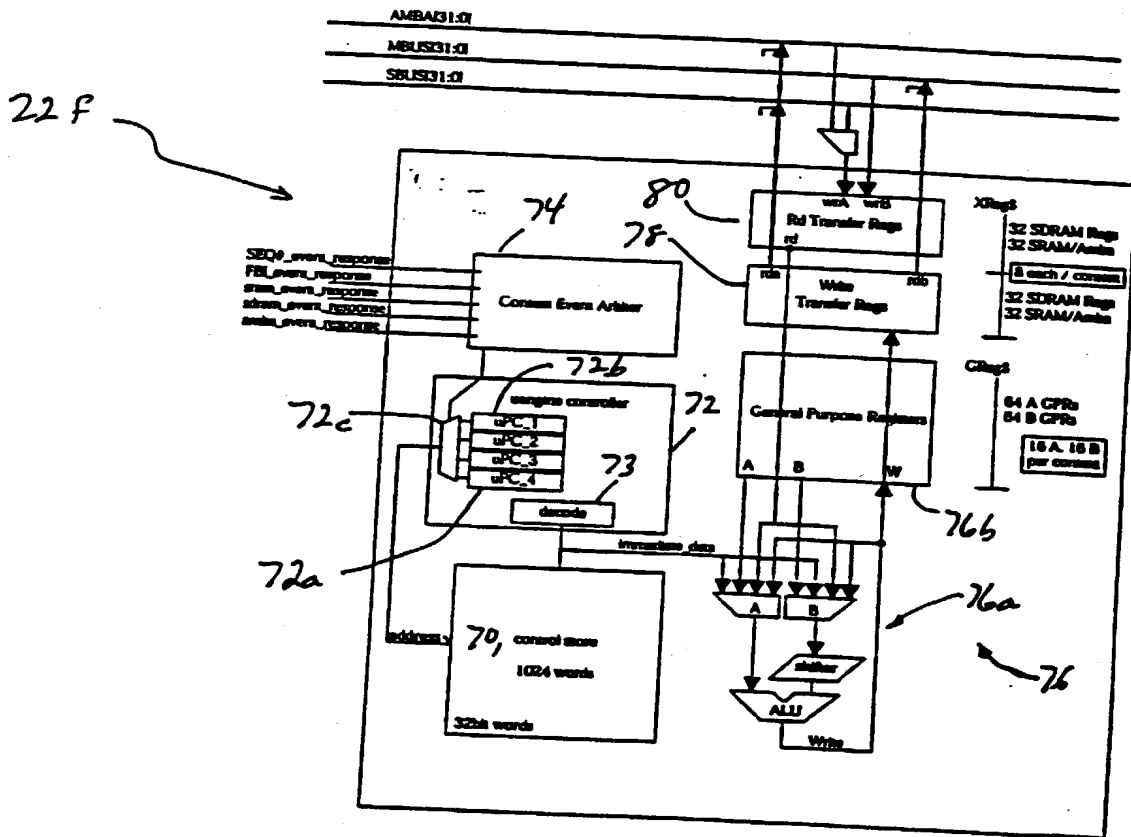


FIG. 3

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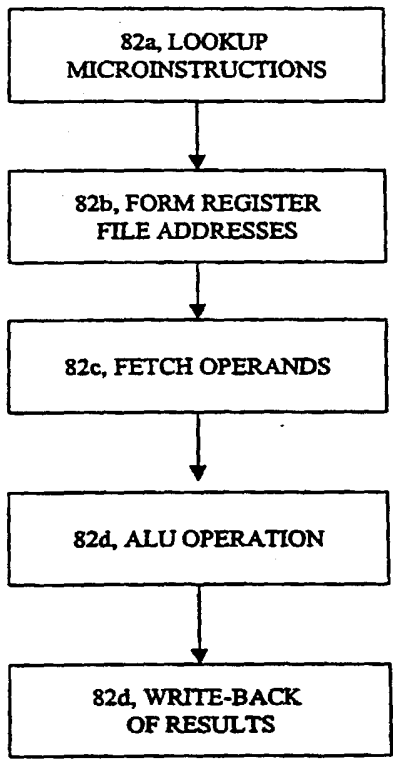


FIG. 4

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branch instruction:

```

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
BRANCH 11 11 11 br mask 1c msk evpip extended br1 Branch Address 1 defbr 1 b1 branch cmd1

```

defbr: A value of 0, 1 or 2 may be specified. If non-zero, the value indicates that the following 1 or 2 microwords will be allowed to execute before the branch operation takes place.

gb: If set, guess that the branch path will be taken, thus prefetch the branch microword address. Otherwise prefetch the non-branch path. This field is only allowed to be set when defbr=0 or defbr=1.

branch address: branch address conditionally or unconditionally selected.

br\_mask: Is decoded to the following options:

- 1) unconditional branch
- 2) branch when  $ALU<31>=1$  ( $<0$ )
- 3) branch when  $ALU<31>=0$  ( $>=0$ )
- 4) branch when  $ALU<31>=1$  OR  $ALU<31:0>=0$  ( $<=0$ )
- 5) branch when  $ALU<31>=0$  AND  $ALU<31:0>!=0$  ( $>0$ )
- 6) branch when  $ALU<31:0>=0$  ( $=0$ )
- 7) branch when  $ALU<31:0>=1$  ( $!=0$ )
- 8) branch when specified context mask = current context
- 9) branch when specified context mask != current context
- 10) branch on carry-out set
- 11) branch on carry-out clear
- 15) look at extended branch field to further decode branch type

extended\_br: branches on various context-swapping signals or other signals.

evpip: indicates pipe stage that this branch should be evaluated in

c\_msk: specifies a context number with which to conditionally branch on.

branch cmd: further specifies the type of branch, e.g., looks at condition codes or some other branch criteria.

FIG. 5A

Matter No.: 10559-307US1

Applicant(s): Gilbert Wolrich et al.

Applicant(s): Gilbert Womack et al.  
**BRANCH INSTRUCTION FOR MULTITHREADED  
 PROCESSOR**

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	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONTEXT	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	wake-up event												ctx end																			

### Context Descriptors

- ```

1) Wake-up Events
   0 = kill
   1 = voluntary
   2 = SRAM
   4 = SDRAM
   8 = FBI
   16 = INTER_THREAD
   32 = PCI_DMA_1
   64 = PCI_DMA_2
   128 = SEQ_NUM_LSB

2) db -> branch defer amount
3) va -> value of sequence number

```

Fig. 5B

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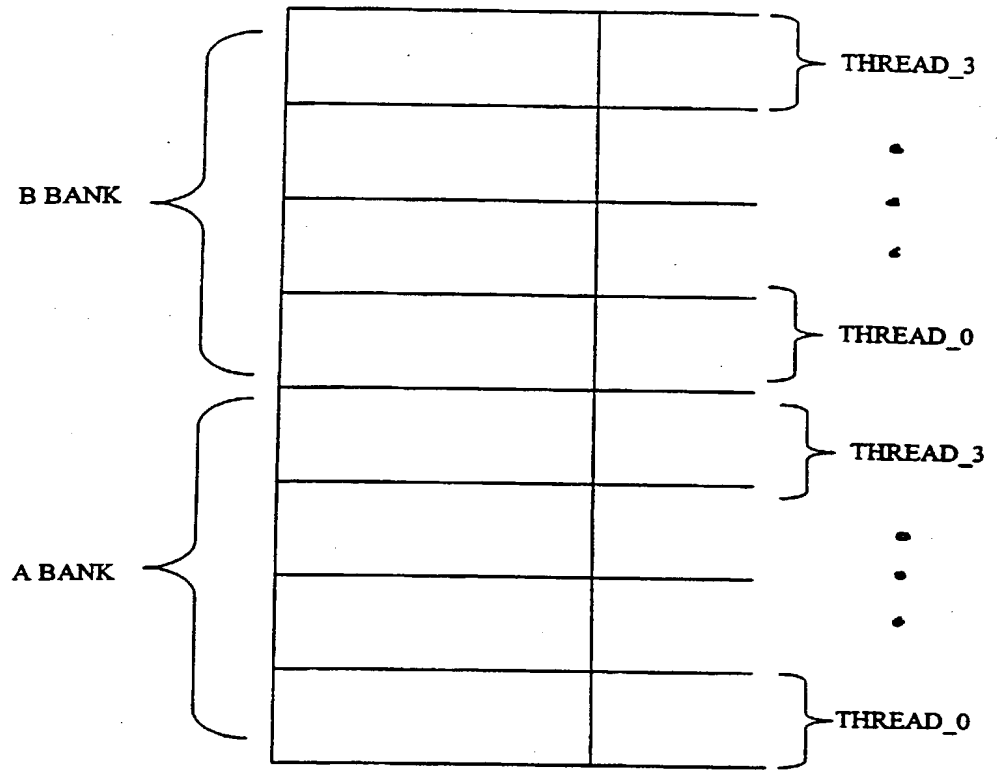


FIG. 6





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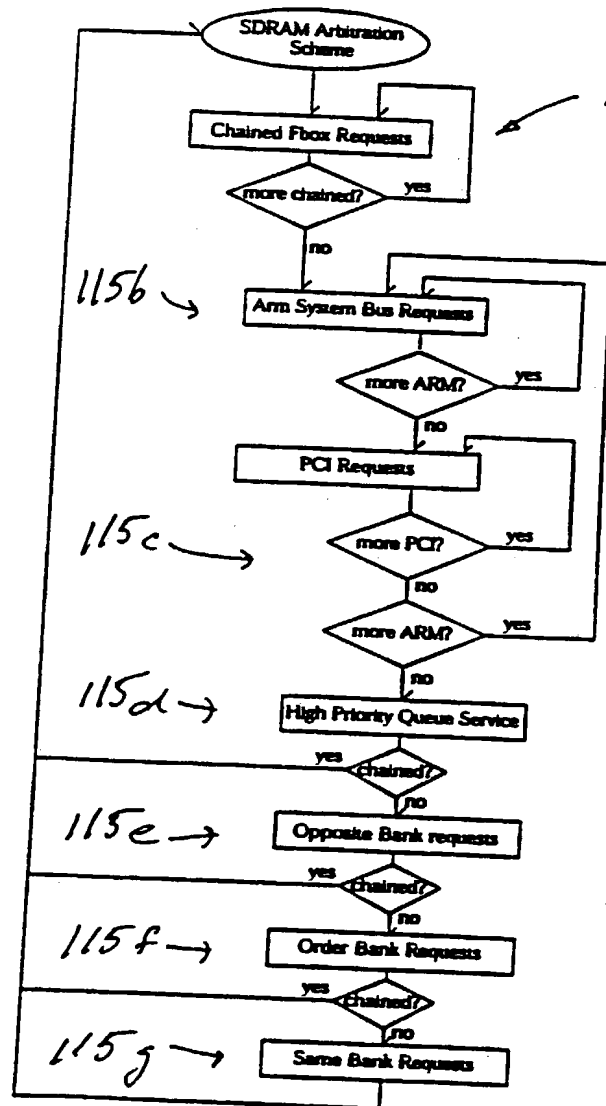


FIG. 7A

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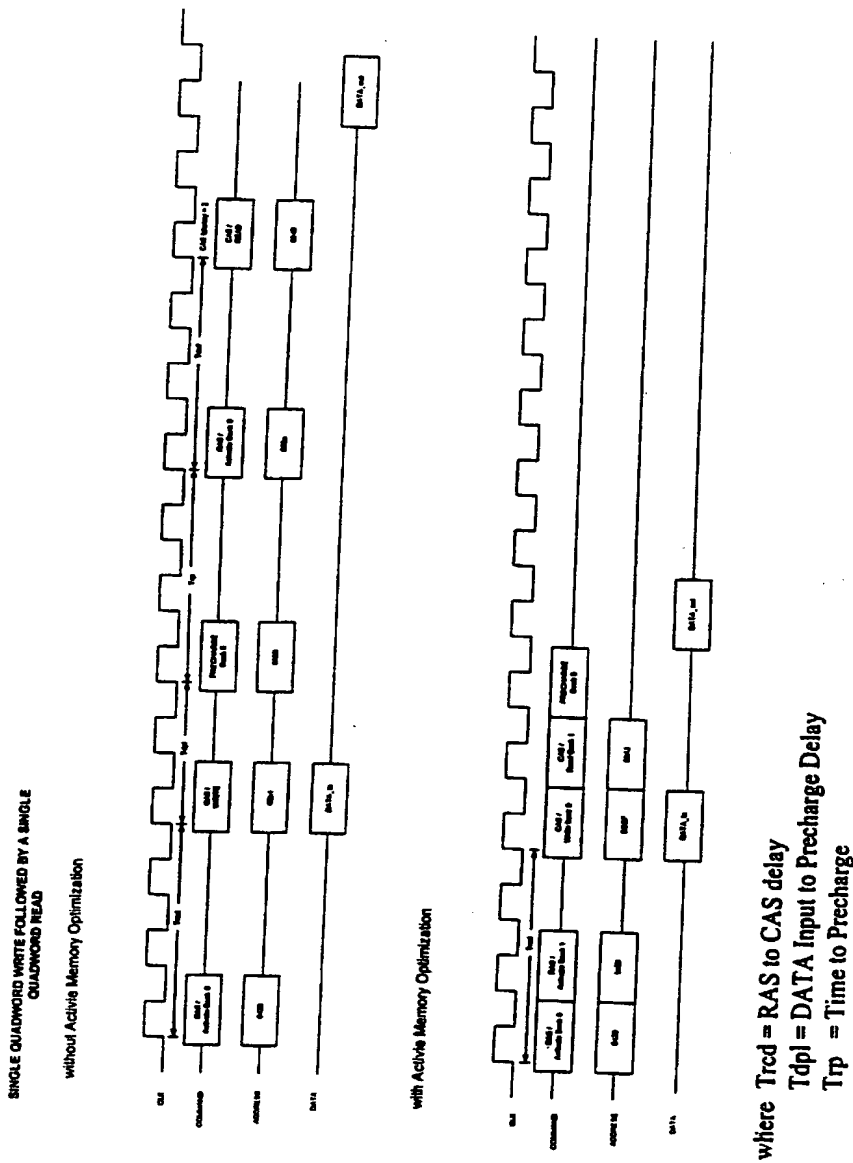


FIG. 7B

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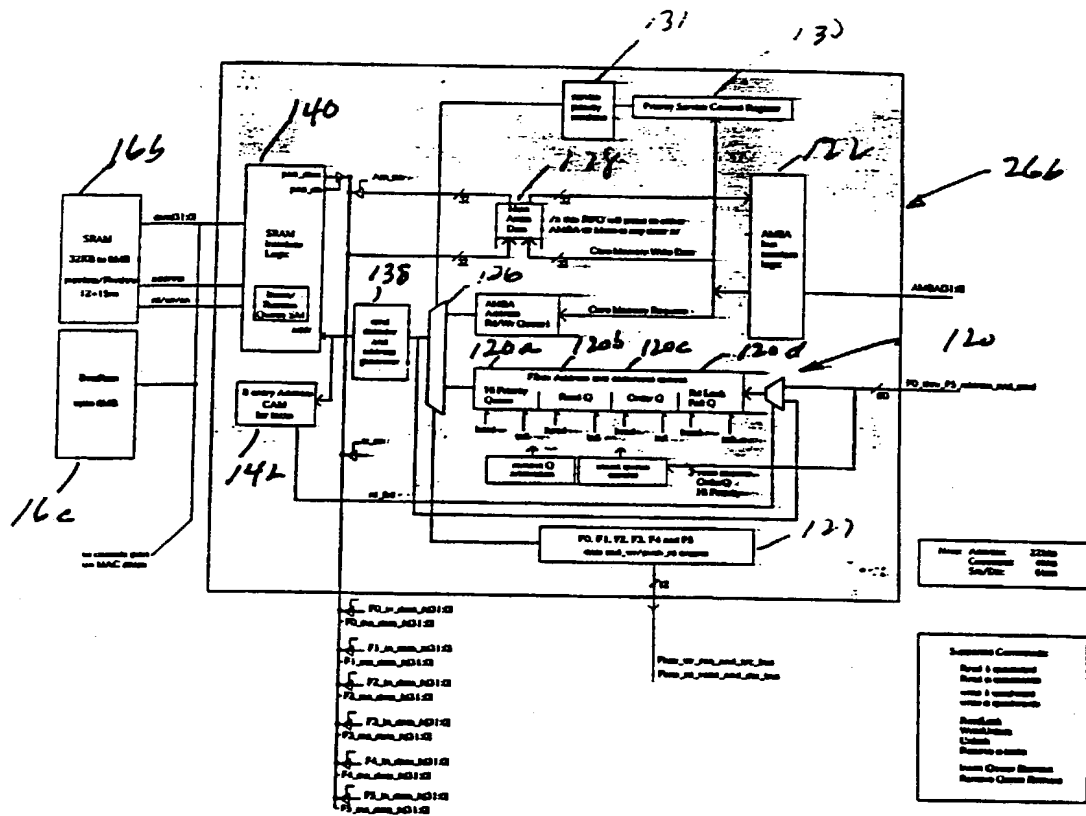
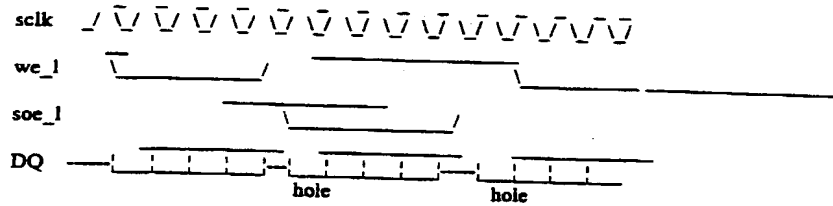


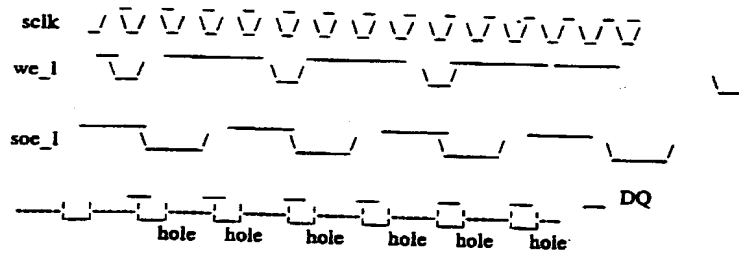
FIG. 8

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4 Writes and 4 Reads followed by more reads with optimization



4 Writes and 4 Reads without optimization



10 cycles vs. 14.

FIG. 8A

